REMARKS

Claims 1-12 were examined. Claims 1-12 were rejected. Claims 1-12 are unchanged. Claims 1-12 remain pending in this application.

The Examiner has rejected claims 1-3 and 10-12 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,233,389 (Barton). Applicant respectfully traverses this rejection.

Independent claim 1 recites:

> An adaptive transport protocol decoder, comprising:
>
> a source of a first stream of packets, each including a payload, and having a first transport protocol;
>
> a source of a second stream of packets, each including a payload, and having a second transport protocol;
>
> a protocol decoder, coupled to the first and second packet stream sources, for extracting the respective payloads from the packets from a selected one of the first and second packet stream sources.

Independent claim 3 was previously dependent from claim 1, but was rewritten in independent form containing all of the limitations of claim 1 and, thus, contains the same recitation.

The adaptive transport protocol decoder recited in claims 1 and 3 includes two sources of packet streams having respectively different transport protocols. Referring to Figure 1 of the present application, a first packet stream source 12 produces packets having the DSS transport packet protocol (format) (originally filed written description: page 4, lines 6-8). A second packet stream source 14 produces packets having the ATSC transport packet protocol (page 4, lines 11-12). One of the two transport packet stream sources is selected by selector 20 (page 4, lines 14-15). The adaptive protocol decoder 30 receives the selected transport packet stream, which has one of two or more different transport protocols. The adaptive protocol decoder 30 performs appropriate processing on the packets in the selected packet stream, adapting that processing depending on the transport protocol of the selected packet stream, to extract the payload data (page 4, lines 18-20). In the case of DSS and ATSC format transport protocol packet streams, the extracted payload data is MPEG2 data, which is decoded by the payload processor 40 (page 4,

lines 25-30). That is, the payload processor 40 decodes MPEG2 data regardless of the transport protocol of the selected transport packet stream (compare to Barton, col. 3, lines 46-52).

Barton does not disclose an adaptive transport protocol decoder including a protocol decoder, coupled to first and a second transport packet stream sources, for extracting the respective payloads from the packets from a selected one of the first and second packet stream sources, having first and second transport protocols, as is recited in claims 1 and 3.

Instead, Barton includes a separate transport protocol decoder for each received signal. This is an example of the very prior art discussed in the present application (written description: page 1, lines 20-28). Referring to Figure 1 of Barton, an input section 101 receives at its input terminal a television stream in one of a plurality of possible formats (col. 3, lines 44-46). If the television signal is in analog form (e.g. NTSC, PAL), it is MPEG encoded (col. 3, lines 49-50). If the television signal is in digital form (e.g. a transport packet stream in DSS, DBS, or ATSC protocol), the input section 101 extracts from the received transport packet stream (e.g. DSS, DBS, ATSC) an MPEG stream representing a selected one of the television signals carried by the received television stream ("The Input Section 101 tunes the channel to a particular program, extracts a specific MPEG program out of it and feeds it to the rest of the system." col. 3, lines 46-49 (emphasis added)). The remainder of the system of Barton operates on an MPEG stream, regardless of the format of the originally received signal (col. 3, lines 46-52).

Referring to Figure 2, Barton discloses more than one Input Section, 201, 202, 203, 204. There is no disclosure that the input sections 201, 202, 203, 204 operate differently than the input section 101 illustrated in Figure . Thus, each of the input sections 201, 202, 203, 204 receives a television stream in one of several possible formats (NTSC, PAL, DSS, DBS, ATSC) and produces an MPEG stream, either from encoding an analog television signal, or by extracting an MPEG signal representing a desired television signal from a digital transport packet stream, as described above.

There is no disclosure of any of the input sections 101 or 201, 202, 203, 204 including an adaptive transport protocol decoder for extracting MPEG payloads from a selected one of two input transport packet streams having respective first and second transport protocols, as is recited in claims 1 and 3.

Applicant respectfully points out that for a reference to anticipate a claim, that reference must disclose every limitation recited in that claim. As described in detail above, Barton does not disclose a protocol decoder, coupled to first and second transport packet stream sources, for extracting the respective payloads from the transport packets from a selected one of the first and second transport packet stream sources, as is recited in independent claims 1 and 3. Barton, thus, cannot be said to anticipate independent claims 1 and 3. For this reason, claims 1 and 3 are deemed allowable over Barton. For the same reasons given above with respect to claims 1 and 3, claims 2, 11, and 12, dependent from claim 1, and claim 10, dependent from claim 3, are also claimed allowable over Barton. However, Applicant makes the following comments on the indicated claims.

Applicant points out that Barton does not disclose any details of the input sections 101, 201, 202, 203, 204. Instead, Barton only discloses that each input section receives a television input stream in one of a plurality of formats (NTSC, PAL, DSS, DBS, ATSC) and produces an MPEG stream representing a television signal carried in that input stream. In general, therefore, Barton cannot be said to disclose details of the adaptive transport protocol decoder.

Claim 2, dependent from claim 1, recites, "The adaptive transport protocol decoder of claim 1 further comprising a selector, having respective input terminals coupled to the first and second packet stream sources, and an output terminal coupled to the protocol decoder ...." As described above with respect to claim 1, Barton does not disclose a protocol decoder operating on a selected one of a first and a second transport packet stream. Thus, Barton cannot disclose a selector having respective input terminals coupled to the first and second transport packet stream sources, and an output terminal coupled to the protocol decoder, as is recited in claim 2.

Independent claim 3 recites, "... the protocol decoder comprises a processor, responsive to a first control program for processing the packets from the first packet stream source to extract the respective payloads, a second control program for processing the packets from the second packet stream source to extract the respective payloads, and a third control program for switching between the first control program and the second control program." Because there is no disclosure of the details of the input sections 101, 201, 202, 203, 204 there can be no disclosure of the input section including a processor for processing packets. Thus, there can be no disclosure of the (non-existent) processor being responsive to a first control program for processing the packets from the first packet stream source to extract the respective payloads, a second control program for

processing the packets from the second packet stream source to extract the respective payloads, and a third control program for switching between the first control program and the second control program, as is recited in claim 3.

Claim 10, dependent from claim 3, recites, "... a selector, having respective input terminals coupled to the first and second packet stream sources, and an output terminal coupled to the protocol decoder, and responsive to a select signal for coupling one of the first and second packet stream sources to the protocol decoder; wherein the third control program is responsive to the select signal to switch to the first control program when the first packet stream source is coupled to the protocol decoder and to switch to the second control program when the second packet stream source is coupled to the protocol decoder." Because there is no disclosure of the internal details of the input sections 101, 201, 202, 203, 204, there can be no disclosure of a selector for coupling one of the first and second packet stream sources to the protocol decoder, as is recited in claim 10. And because, as described above with respect to claim 3, there is no disclosure in Barton of a processor responsive to a first, second and third control program, there can be no disclosure that the third control program switching the processor to the first or second control program in response to the select signal, as is recited in claim 10.

With respect to claims 1-2 and 11-12, the Examiner contends that Barton discloses in the input section 101 a protocol decoder for extracting payloads from packets of a select transport packet stream. However, Barton does not disclose any details about the input section 101. Instead, input section 101 is represented as a black box which receives input television transport signals in a plurality of formats, and produces an MPEG signal representing one television signal.

First, applicant contends that the disclosure in Barton describing the input section 101 does not necessarily imply that the input section 101 simultaneously receives a plurality of input television signals in two or more of the possible formats (NTSC, PAL, DSS, DBS, ATSC), as suggested by the Examiner. Applicant, instead, contends that input section 101 receives a single television transport signal in one of the plurality of possible formats, and produces an MPEG signal representing that television signal, or, in digital formats, one of a plurality of transport multiplexed television signals.

Second, even if the input sections 101, 201, 202, 203, 204 in Barton are considered to simultaneously receive a plurality input television signals, and in particular multiple digital

transport packet streams having respectively different transport packet protocols, there is still no disclosure that the input section 101, 201, 202, 203, 204 contains an adaptive protocol decoder which extracts respective payloads from a selected one of the received transport packet streams, as is recited in claims 1 and 3. Instead, the prior art provides the same function by using a plurality of separate digital television signal transport protocol decoders. Each such decoder is designed to receive a transport packet stream in one protocol (DSS, DBS, ATSC), to extract the payload from the packets in that stream, and to produce a payload signal, in this case an MPEG stream. A desired MPEG stream, and possibly a desired television program from within the stream, is selected and produced at the output of the input section 101, 201, 202, 203, 204. Thus, the input section 101 could as easily been designed according to the prior art described in the present application by including one transport decoder for each received signal.

Because there is no explicit disclosure of the design and implementation of the input section 101 of Barton, and because there is a prior art design and implementation which would provide the disclosed function of the input section 101, the Examiner cannot say, therefore, that the input section 101 anticipates the invention recited in claim 1

With respect to claims 3 and 10, the Examiner contends that the protocol decoder of Barton has an inherent processor and inherent control programs to select and decode the packets of different formats and change the type of decoding performed. Applicant disagrees. As described above, input sections 101, 201, 202, 203, 204 are disclosed as black boxes receiving television streams in a plurality of different formats at their input and producing an MPEG stream representing a selected television program at their output. There is no disclosure, in either the drawing or the associated written description, of the internal details of the input sections 101, 201, 202, 203, 204, and in particular, no disclosure of a processor and control programs. In fact, Barton emphasizes that prior art systems using a processor to compress and store video data are difficult to implement because the processor requirements for keeping up with the high video rates makes such a device expensive and problematic (col. 1, lines 45-49). Instead, the Barton system can move large quantities of information with minimal intervention by the CPU (col. 6, lines 21-25). Barton, thus, teaches away from using a processor to decode transport packets. In view of this, it would not be reasonable to conclude that Barton inherently discloses a processor responsive to control programs in the input sections 101, 201, 202, 203, 204 to process video data, as contended by the Examiner.

In addition, one skilled in the art will understand that there is an equivalence between implementing a function in hardware and with a processor responsive to control programs. The functions disclosed in Barton may be implemented by a wide range of technology: e.g. discrete components, SSI, MSI, LSI, VLSI, PLA integrated circuits in addition to a processor. Any of these technologies, or a combination of two or more of them, may be used for a variety of design criteria. In view of the wide variety of technologies, designs and implementations which may provide the functions disclosed in Barton, applicant disagrees that a processor is inherent in the input sections 101, 201, 202, 203, 204.

For the reasons given above, independent claims 1 and 3 are deemed allowable over Barton. For the same reasons given above with respect to claims 1 and 3, claims 2, 11 and 12, dependent from claim 1, and claim 10, dependent from claim 3, are also deemed allowable over Barton. The Examiner is respectfully requested to reconsider and withdraw this rejection.

The Examiner has also rejected claims 4-9 under 35 U.S.C. § 103(a) as being unpatentable over Barton, as applied to claim 3, and further in view of U.S. Patent 5, 410,709 (Yu). Applicant respectfully traverses this rejection.

Claim 3 recites in pertinent part,

> ... a protocol decoder, coupled to the first and second packet stream sources, for extracting the respective payloads from the packets from a selected one of the first and second packet stream sources;
>
> wherein the protocol decoder comprises a processor, responsive to a first control program for processing the packets from the first packet stream source to extract the respective payloads, a second control program for processing the packets from the second packet stream source to extract the respective payloads, and a third control program for switching between the first control program and the second control program.

Claim 4, dependent from claim 3, recites in pertinent part,

... both of the first and second control programs comprise:

a packet handler, executed in response to each received packet;

a plurality of interrupt drivers, stored in the memory at respective locations, called by software interrupt;

an interrupt vector, stored at a fixed, predetermined location in memory, including a plurality of entries, each containing a pointer to a respective location of an interrupt driver.

As described in detail above, Barton does disclose input sections 101, 201, 202, 203, 204 each of which receives a television input stream, possibly in the form of a transport packet stream, and produces an MPEG stream representing a television signal carried by the payloads in the received transport packet stream. However, Barton does not disclose or suggest any details of the implementation of the input sections 101, 201, 202, 203, 204. Thus, Barton cannot disclose or suggest that the input sections 101, 201, 202, 203, 204 include a protocol decoder for extracting the payloads from packets from a selected one of a first and second transport packet streams; nor that the protocol decoder includes a processor, responsive to a first control program for processing the packets from the first packet stream source to extract the respective payloads, a second control program for processing the packets from the second packet stream source to extract the respective payloads, and a third control program for switching between the first control program and the second control program, as recited in claim 3. In fact, as described above, Barton teaches away from using a processor to process packets due to the high speed requirements for such a processor (col. 1, lines 45-49; col. 6, lines 21-25).

Because Barton does not disclose or suggest a processor responsive to first, second and third control programs in the input sections 101, 201, 202, 203, 204, it cannot disclose or suggest that both of the first and second control programs comprise a packet handler, executed in response to each received packet, a plurality of interrupt drivers, stored in the memory at respective locations, called by software interrupt, nor an interrupt vector, stored at a fixed, predetermined location in memory, including a plurality of entries, each containing a pointer to a respective location of an interrupt driver, as recited in claim 4.

Yu does not disclose or suggest an adaptive transport protocol decoder, nor a first and second source of transport packet streams having respectively different transport protocols, nor a protocol decoder, coupled to the first and second packet stream sources, for extracting payloads from a selected one of the first and second packet stream sources, nor that the (non-existent) protocol decoder includes a processor, responsive to a first control program for processing the packets from the first packet stream source to extract the respective payloads, a second control program for processing the packets from the second packet stream source to extract the respective payloads, and a third control program for switching between the first control program and the second control program, as recited in claim 3.

Because Yu does not disclose or suggest protocol decoder with a processor responsive to first and second and third control programs, it cannot disclose or suggest that both of the first and second control programs comprise a packet handler, executed in response to each received packet, nor a plurality of interrupt drivers called by software interrupt, as recited in claim 4.

Instead, Yu discloses a dual processor system for handling terminal communications involving a large number of communications terminals. Referring to Figure 1, the communications terminals (not shown) are coupled to the dual processor system 12, 14, 16, 18 via peripheral controllers 20-1, 20-2 ... 20-n (col. 3, lines 14-22). One of the two processors 12, 14 in the dual processor system controls communications with any particular communications terminal at any particular time, but control of that communications terminal may pass from one processor to the other (col. 4, lines 12-17). A communications terminal requests service from its processor by issuing a hardware interrupt which is passed from the peripheral controller 20-1, 20-2 ... 20-n to the operating system of the processor 12, 14 controlling that communications terminal (col. 4, lines 10-12 and 26-32, col. 6, lines 41-43). Yu discloses a system for updating the interrupt system so that the each processor 12, 14 receives hardware interrupts from the communications terminals it is controlling (col. 4, lines 26-32). Referring to Figure 2b, Yu also discloses a plurality of interrupt drivers (14-4) and an interrupt vector table 42, including a plurality of entries (CHAN. 0, CHAN. 1, etc.) containing a pointer (Interrupt Handler Pointer) to a location of an interrupt handler routine 14-4 (col. 5, lines 17-19, lines 42-44). An appropriate interrupt handler routine 14-4 is invoked in response to receipt of a hardware interrupt from one of the communications terminal.

First, applicant contends that there is no motivation to combine Barton with Yu. Applicant respectfully points out that before references may be combined and applied to a claim, those

references must provide a motivation leading to the combination, and that motivation may not come from the application containing the claim against which those references are applied. As described above, Barton does not disclose or suggest that the input sections include a processor. Thus, there would be no reason for one skilled in the art, when considering Barton, to search processor related art to provide the functions disclosed for the input sections: receiving a television stream and producing an MPEG stream representing a selected television program. In fact, as described above, Barton teaches away from the use of processors to provide such high speed video functions. Yu is not related to video processing in any way. Thus, there would be no reason for one skilled in the art, when considering Yu, to search video processing related art for any reason. Consequently, neither reference provides any motivation to be combined with the other in the manner suggested by the Examiner. The only motivation the Examiner has for combining Barton with Yu is applicant's own teachings showing the use of the interrupt function of a processor for extracting payloads from a selected one of two transport packet streams having different transport protocols. This, however, is impermissible hindsight.

Second, even if the references are combined, as suggested by the Examiner, Applicant contends that the combination would not render the invention recited in claim 4 unpatentable. Applicant respectfully points out that before a claim may be rendered unpatentable by a combination of references, that combination of references must disclose or suggest every limitation of that claim. As described above, neither Barton nor Yu disclose or suggest a protocol decoder, coupled to the first and second packet stream sources, for extracting the respective payloads from the packets from a selected one of the first and second packet stream sources. Because neither Barton nor Yu disclose such a protocol decoder, they cannot disclose or suggest that the protocol decoder includes a processor responsive to a first control program for processing the packets from the first packet stream source to extract the respective payloads, a second control program for processing the packets from the second packet stream source to extract the respective payloads, and a third control program for switching between the first control program and the second control program, all as recited in claim 3.

Further, because neither Barton nor Yu disclose such a protocol detector including a processor responsive to first, second and third control programs, they cannot disclose that both of the first and second control programs comprise a packet handler, executed in response to each received packet, a plurality of interrupt drivers, stored in the memory at respective locations, called

by software interrupt, nor an interrupt vector, stored at a fixed, predetermined location in memory, including a plurality of entries, each containing a pointer to a respective location of an interrupt driver, as is recited in claim 4. Because the combination of Barton and Yu does not disclose or suggest every limitation of claim 4, it cannot be said to render claim 4 unpatentable. Claim 4, therefore, is deemed allowable over Barton in view of Yu. Claims 5-9, ultimately dependent from claim 4 are deemed allowable for the same reasons given above with respect to claim 4. However applicant makes the following comments about the indicated claims.

Claim 5, dependent from claim 4, recites in pertinent part, "... the third control program switches between the first and second control programs by moving the interrupt vector of one of the first and second control programs to the fixed predetermined location in the memory, and simultaneously moving the interrupt vector of the other one of the first and second control programs to another location in the memory." As described above, Barton does not disclose or suggest a processor in the input sections, so it cannot disclose or suggest details of the operation of a control program operating on the (non-existent) processor. Yu does disclose an interrupt vector 42. However, this interrupt vector 42 is constructed at boot up time (col. 6, lines 16-20). There is no disclosure or suggestion that the interrupt vector 42 is swapped with another interrupt vector stored in a different location in memory, as recited in claim 5. Because neither Barton nor Yu disclose swapping interrupt vectors, claim 5 is deemed allowable over Barton in view of Yu.

Claim 6, dependent from claim 4, recites, in pertinent part, "... both the first and second control programs further comprise a buffer for storing the respective extracted payloads at a location in the memory." Claim 7, dependent from claim 6, recites, in pertinent part, "... the third control program switches between the first and second control programs by moving the interrupt vector of one of the first and second control programs to the fixed predetermined location in the memory, and simultaneously moving the interrupt vector of the other one of the first and second control programs to another location in the memory; and reallocating the buffer to a location in the memory." As described above, Barton does not disclose or suggest a processor in the input sections, so it cannot disclose or suggest details of the operation of a control program operating on the (non-existent) processor. Yu does not disclose or suggest the presence of a buffer for containing payloads, and, thus, cannot disclose or suggest reallocating the buffer when switching between the first and second control programs, as recited by claim 7. Claims 6 and 7, thus, are deemed allowable over Barton in view of Yu.

For the reasons given above, applicant deems claims 4-10 allowable over Barton in view of Yu. The Examiner is respectfully requested to reconsider and withdraw this rejection and allow claims 4-10.

In view of the above amendments and arguments, claims 1-12 are deemed allowable. The Examiner is respectfully requested to reconsider and withdraw the rejections, and to allow the amended application.

Respectfully submitted,

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Date: August 5, 2004

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August 5, 2004
Date

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